IN THE SPECIFICATION

Please replace paragraph [0033] of the published application with the following amended paragraph [0033]:

[0033] FIG. 7 is a diagram showing a configuration of the shift register 14, according to the first embodiment. The shift register 14 shown in FIG. 7 includes switches SW0 through SW3, flip-flops FF0 through FF3 and FF1' through FF3', inverters 30 trough 33, and NOR gates 34 through 37. The input-point selector 12 outputs a signal selecting the column N1 of the shift register 14 to the shift register 14 by following the address signal A2 after receiving the address signal A2 and the data-write command as shown in FIG. 6A. To be concrete, the input-point selector 12 outputs a high-level signal from its output terminal N(A2) to the switch SW2 of the shift register 14, and low-level signals from the other terminals N(A0), N(A1) and N(A3) respectively to the switches SW0, SW1 and SW3. The switch SW2 connects to a side "b" after receiving the high-level signal from the output terminal N(A2) of the input-point selector 12. Each of the switches SW1 ~~SW0~~ and SW3 connects to a side "a" after receiving the low-level signal respectively from the output terminals N(A1) ~~N(A0)~~ and N(A3) of the input-point selector 12. Additionally, the switch SW0 becomes disconnected after receiving the low-level signal from the output terminal N(A0) of the input-point selector 12.

ok to enter
JB
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